What is claimed is:

1. A testing circuit comprising:

m (m is an integer of 2 or more) block test units, each of which compares a first data of n (n is a positive integer) bits with a reference data of said n bits for each corresponding bit, and outputs a comparison result as a test circuit output signal based on a output control signal, wherein said first data is outputted from corresponding one of m object circuits for a test; and

a first logical processing unit which judges whether or not said all of m said test circuit output signals indicate that said first data is coincident with said reference data, and outputs a judgment result as a total judgment result signal based on said m test circuit output signals,

wherein each of said m block test units includes:

a block judging unit which compares said first data with said reference data for each corresponding bit to judge whether said first data is coincident with said reference data, and outputs a comparison result as a block judgment result signal, and

a block output selecting unit which outputs one of said block judgment result signal and a predetermined standard signal as said test circuit output signal based on said output control signal.

2. The testing circuit according to claim 1, wherein said output control signal is set such that said block output selecting unit outputs one of said block judgment result signal and said standard signal, in reference to a test condition for said one of m object circuits when said first data is outputted.

3. The testing circuit according to claim 2, wherein said block output selecting unit outputs said block judgment result signal when said test condition corresponds to said one of m object circuits, and outputs said standard signal when test condition does not correspond to said one of m object circuits, based on said output control signal.

4. The testing circuit according to claim 2 or 3, wherein said standard signal is set as the same logical state of said block judgment result signal indicating that said first data is coincident with said reference data.

5. The testing circuit according to any one of claims 1 to 4, wherein said total judgment result signal indicates all of said m object circuits pass said test, in case that all of m said test circuit output signal indicate that said first data is coincident with said reference data.

6. The testing circuit according to any one of claims 1 to 5, wherein said total judgment result signal indicates at least one of said m object circuits fails said test, in case that at least one of m said test circuit output signal indicates that said first data is not coincident with said reference data.

7. The testing circuit according to any one of claims 1 to 6, wherein said block judging unit includes:

n individually judging units, each of which compares one of n bits of said first data with corresponding one of n bits of said reference data, and outputs a comparison result as a comparison result signal, and

a second logical processing unit which outputs said block judgment result signal indicating whether or not said first data is coincident with said reference data, based on a plurality of said comparison result signals supplied from said n individually judging units.

8. The testing circuit according to claim 7, wherein said block judgment result signal indicates that said first data is coincident with said reference data, in case that all of said comparison result signals indicate that said one of n bits of the first data is

coincident with said corresponding one of n bits of the reference data.

9. A semiconductor device comprising:

m (m is an integer of 2 or more) memory macros, each of which includes a plurality of non-volatile memory cells that are electrical erasable and writable;

a testing unit which carries out an erasing verifying test and a writing verifying test that are tests verifying of results of a erasing operation and a writing operation to said memory cell, respectively; and

a test output terminal which outputs test results carried out by said testing unit to an outside,

wherein a memory size of at least one of said m memory macros is different from that of another, said memory size corresponds to a number of said memory cell,

said testing unit tests said m memory macros in parallel.

10. The semiconductor device according to claim 9, wherein said testing unit includes:

m comparison judging units, each of which is installed correspondingly to one of said memory macros, compares a first data of a plurality of bits outputted

from corresponding one of said memory macros with a reference data of said plurality of bits for each corresponding bit to judge whether said first data is coincident with said reference data, and outputs a comparison result as a first judgment signal,

m first selecting units, each of which is installed correspondingly to one of said comparison judging units, and outputs one of said first judgment signal and a predetermined standard signal as a second judgment signal based on an output control signal, said first judgment signal is supplied from corresponding one of said comparison judging units, and

a totally judging unit which judges whether or not said all of m said second judgment signals indicate that said first data is coincident with said reference data, and outputs a judgment result as a total judgment result signal based on said m second judgment signals.

11. The semiconductor device according to claim 10, wherein said output control signal is set based on whether or not a memory cell corresponding to an address exists in said memory macro,

said address is commonly supplied to said m memory macros as an address signal when one of said erasing verifying test and said writing verifying test is carried out to said memory macro.

12. The semiconductor device according to claim 11, wherein said output control signal is set such that said first selecting unit outputs said first judgment signal when said memory cell corresponding to said address exists in said memory macro.

13. The semiconductor device according to claim 11 to 12, wherein said standard signal is set as the same logical state of said first judgment signal indicating that said first data is coincident with said reference data.

14. The semiconductor device according to any one of claims 11 to 13, wherein said total judgment result signal indicates all of said m memory macros pass said test, in case that all of m said second judgment signals indicate that said first data is coincident with said reference data.

15. The semiconductor device according to any one of claims 11 to 14, wherein said total judgment result signal indicates at least one of said m memory macros fails said test, in case that at least one of m said second judgment signals indicates that said first data is not coincident with said reference data.

16. The semiconductor device according to any one of claims 10 to 15, wherein said reference data indicates a data which includes at least pattern data corresponding to an erasing verifying test and a writing verifying test, respectively.

17. The semiconductor device according to any one of claims 10 to 16, further including:

a memory unit which stores data of a plurality of said reference data and outputs one of said reference data when one of said erasing verifying test and said writing verifying test is executed.

18. The semiconductor device according to claim 17, further including:

a second selecting unit which selects said reference data from said plurality of reference data in said memory unit, corresponding to a type of a verifying test to be executed, and outputs said reference data to said each of m comparison judging units.

19. The semiconductor device according to any one of claims 10 to 18, wherein said comparison judging unit includes:

a plurality of coincident judging units, each of which compares one of said plurality of bits of said

first data with corresponding one of said plurality of bits of said reference data, and outputs a comparison result; and

a logical unit which outputs said first judgment signal indicating whether or not said first data is coincident with said reference data based on a plurality of said comparison results supplied from said plurality of coincident judging units.

20. The semiconductor device according to claim 19, wherein said first judgment signal indicates that said first data is coincident with said reference data, in case that all of said comparison results of said plurality of coincident judging units indicate that said one of the plurality of bits of the first data is coincident with said corresponding one of the plurality of bits of the reference data.

21. The semiconductor device according to any one of claims 9 to 20, further comprising:

a CPU;

a testing address input terminal;

a third selecting unit which selectively outputs a CPU address signal supplied from said CPU at the time of usual operations or a testing address signal supplied through said testing address input terminal at the time of verifying tests as a first address

signal, based on a test mode signal that is activated at the time of said verifying tests; and

a decoder unit which decodes said first address signal, and outputs a second address signal for said memory macro and said first enable signals that indicate which of said respective memory macros is an access target.

22. The semiconductor device according to claim 21, further comprising:

a fourth selecting unit which selectively outputs a CPU data signal supplied from the CPU at the time of said usual operations or a testing data signal supplied through a testing data input terminal at the time of said verifying tests based on said test mode signal.

23. A semiconductor device comprising:

a first memory macro which includes a first memory size;

a second memory macro which includes a second memory size larger than said first memory size;

a first comparing unit which outputs a first coincident signal in case that a first test data read out from said first memory macro is coincident with an first expectation data, and a first inconsistency signal in case that said first test data is not

coincident with said first expectation data;

a second comparing unit which outputs a second coincident signal in case that a second test data read out from said second memory macro is coincident with a second expectation data, and a second inconsistency signal in case that said second test data is not coincident with said second expectation data; and

a gate unit which outputs a third coincident signal in case when receiving said first coincident signal from said first comparing unit and said second coincident signal from second comparing unit.

24. A testing method for a semiconductor device, comprising:

supplying an address signal indicating an address to one of m (m is an integer of 2 or more) memory macros to obtain a first data stored in a memory cell corresponding to said address, wherein said address is commonly supplied to said m memory macros;

comparing said first data of a plurality of bits outputted from said one of m memory macros with a reference data of said plurality of bits for each corresponding bit to judge whether said first data is coincident with said reference data, and generating a comparison result as a first judgment signal, for all said m memory macros;

selecting one of said first judgment signal and

a predetermined standard signal as a second judgment signal based on an output control signal, for said all m memory macros;

judging whether or not said all of m said second judgment signals indicate that said first data is coincident with said reference data; and

generating a total judgment result signal which indicates a judgment result,

wherein said output control signal is set based on whether or not said memory cell corresponding to said address exists in said one of m memory macros.

25. The testing method for a semiconductor device according to claim 24, wherein said output control signal is set such that said first judgment signal is selected when said memory cell corresponding to said address exists in said one of m memory macros.

26. The testing method for a semiconductor device according to claim 25, wherein said standard signal is set as the same logical state of said first judgment signal indicating that said first data is coincident with said reference data.

27. The semiconductor device according to claim 25 or 26 , wherein said total judgment result signal indicates all of said m memory macros pass said test,

in case that all of m said second judgment signals indicate that said first data is coincident with said reference data.

28. The semiconductor device according to claim any one of 25 to 27, wherein said total judgment result signal indicates at least one of said m memory macros fails said test, in case that at least one of m said second judgment signals indicates that said first data is not coincident with said reference data.

29. The testing method for a semiconductor device according to any one of claims 25 to 28, wherein said comparing step includes:

comparing one of said plurality of bits of said first data with corresponding one of said plurality of bits of said reference data; and

generating said first judgment signal indicating whether or not said first data is coincident with said reference data based on a plurality of said comparison results.

30. The testing method for a semiconductor device according to claim 29, wherein said first judgment signal indicates that said first data is coincident with said reference data, in case that all of said comparison results of said plurality of coincident

judging units indicate that said one of the plurality of bits of the first data is coincident with said corresponding one of the plurality of bits of the reference data.

31. A computer program product embodied on a computer-readable medium and comprising code that, when executed, causes a computer to perform the following:

supplying an address signal indicating an address to one of m (m is an integer of 2 or more) memory macros to obtain a first data stored in a memory cell corresponding to said address, wherein said address is commonly supplied to said m memory macros;

comparing said first data of a plurality of bits outputted from said one of m memory macros with a reference data of said plurality of bits for each corresponding bit to judge whether said first data is coincident with said reference data, and generating a comparison result as a first judgment signal, for all said m memory macros;

selecting one of said first judgment signal and a predetermined standard signal as a second judgment signal based on an output control signal, for said all m memory macros;

judging whether or not said all of m said second judgment signals indicate that said first data is

coincident with said reference data; and

generating a total judgment result signal which indicates a judgment result,

wherein said output control signal is set based on whether or not said memory cell corresponding to said address exists in said one of m memory macros.

32. The computer program product according to claim 31, wherein said output control signal is set such that said first judgment signal is selected when said memory cell corresponding to said address exists in said one of m memory macros.

33. The computer program product according to claim 32, wherein said standard signal is set as the same logical state of said first judgment signal indicating that said first data is coincident with said reference data.

34. The computer program product according to claim 32 or 33, wherein said total judgment result signal indicates all of said m memory macros pass said test, in case that all of m said second judgment signals indicate that said first data is coincident with said reference data.

35. The computer program product according to any one

of claims 32 to 34, wherein said total judgment result signal indicates at least one of said m memory macros fails said test, in case that at least one of m said second judgment signals indicates that said first data is not coincident with said reference data.

36. The computer program product according to any one of claims 32 to 35, wherein said comparing step includes:

comparing one of said plurality of bits of said first data with corresponding one of said plurality of bits of said reference data; and

generating said first judgment signal indicating whether or not said first data is coincident with said reference data based on a plurality of said comparison results.

37. The computer program product according to claim 36, wherein said first judgment signal indicates that said first data is coincident with said reference data, in case that all of said comparison results of said plurality of coincident judging units indicate that said one of the plurality of bits of the first data is coincident with said corresponding one of the plurality of bits of the reference data.